

ABSTRACT

A scheme to reduce clock jitter is disclosed in applications where video content is transmitted through multiple stages, each having a switch allowing that stage's video stream to be selected. The video data is re-clocked using a new clock at each stage. Before re-clocked, the video data from the preceding stage is scaled into a constant resolution using a digital scaler. Since the downstream stages could re-clock the video as if it were sent at the same frequency, there is no need to anticipate the changeable video frequency and to create the necessary low-jitter clock in programmable logic.

TECHNICAL ABSTRACT